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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/600,245
Filing Date: June 20, 2003
Appellant(s): BHATIA, SANDEEP

Kirk A. Vander Leest
Registration No. 34,036
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/16/2011 appealing from the Office action mailed 12/13/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

1-11, 16-26.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN

REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

US 7,130,526	Abelard et al.	10-2006
US 6,353,700	Zhou	03-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 5, 8, 11, and 22-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. "**a forward order of display at normal speed**" is not disclosed anywhere in the specification; and "**every picture** is displayed" is not disclosed in the specification; "wherein

the queue directly transmits the indicators from the first processor to the second processor" is not disclosed in the specification.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-11, 16-21, and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Abelard et al. (US 7,130,526).

Re claims 1 and 5, Abelard discloses a system for displaying images on a display (fig. 1), said system comprising:

a decoder (9 of fig. 1, a video decoder, col. 4, lines 14-20) for decoding encoded images and parameters associated with the images (DECODING MANAGER of fig. 1, there are parameters for decoding as shown in figure 5, I, B, P parameters), thereby resulting in decoded images and decoded parameters associated with the decoded images (26 of fig. 1, A, B, and C are decoded memories to store the decoded image and the decoded parameters, fig. 7, A memory stored I2, P8, B"1, B"0, P5, B9, P5, I'2, P'2, P'8, B1, B0 accordance to decoding per frame period);

image buffers (26 of fig. 1, A, B, C are decoded image buffers) for storing the decoded images;

a FIFO (DISPLAY MANAGER of fig. 2, col. 5, lines 37-42; col. 5, lines 43-col. 6, line 10; fig. 3) for storing indicators (the descriptors are shared by the decoding manager and the display manager, col. 5, lines 43-46) indicating images to be displayed (col. 6, lines 39-51, identifying the next picture to be displayed; col. 6, lines 66-col. 7, line 3) in a forward display order at normal speed (col. 6, lines 66-col. 7, line 3; note In forward mode, Next(N) returns the ID of following picture to be displayed according to normal display order (i.e. in respect to the temporal reference). In backward mode. Next(N) returns the ID of the previous picture according to normal display order); and

a display engine (14 of fig. 1) for presenting the images indicated by the FIFO for display.

Re claims 2 and 6, Abelard further discloses the A, B, and C buffers (26 of fig. 1) buffer inherently has parameter buffers for storing the decoded parameters (I, B, P parameters as shown in figure 5) associated with the images (e.g. I, B, and P picture).

Re claims 3 and 7, Abelard further discloses wherein the display engine (14 of fig. 1) presents the images indicated by the queue for display by receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

Re claim 4, Abelard further discloses wherein the decoder comprises a first processor (9 of fig. 1)and the display engine comprises a second processor (14 of fig. 1).

Re claim 8, Abelard discloses a circuit (fig. 1) for displaying images on a display (14 of fig. 1), said circuit comprising:

a processor (10 fig. 1);

a memory (24 of fig. 1) operably coupled to the processor,

said memory storing a plurality of executable instructions (col. 4, lines 21-24),

wherein the plurality of executable instructions (figs. 2-6) cause:

decoding encoded images and parameters associated with the images (figs. 3 and 5), thereby resulting in decoded images and decoder parameters associated with the decoded images (fig. 4);

storing the decoded images (26 of fig. 1);

storing indicators indicating images to be displayed in a FIFO (DISPLAY MANAGER of fig. 2, note the Display Manager checks every 40 ms which picture is to be displayed. In other words, it identifies the reconstruction buffer containing the picture to be displayed, Col. 5, line 54-col.6, line 20) in a forward display order at normal speed (col. 6, lines 66-col. 7, line 3; note In forward mode, Next(N) returns the ID of following picture to be displayed according to normal display order (i.e. in respect to the temporal reference). In backward mode. Next(N) returns the ID of the previous picture according to normal display order); and

presenting the images indicated by the stored indicators for display (14 of fig. 1, see fig. 3).

Re claim 9, Abelard further discloses storing the decoded parameters (I, B, P parameters as shown in figure 5) associated with the images (A, B, and C of fig. 7).

Re claim 10, Abelard further discloses wherein the instructions causing presenting the images further comprise instructions causing receiving the decoded parameters and displaying the decoded images based on the decoded parameters (fig. 3).

Re claim 11, Abelard further discloses a circuit (fig. 1) for displaying images on a display, said circuit comprising:

a first processor (10 of fig. 1);

a first memory (24 of fig. 1) operably coupled to the first processor,

said first memory storing a plurality of instructions for execution by the first processor (col. 4, lines 21-24),

wherein the plurality of executable instructions cause (Note Receiver 1 also comprises a reprogrammable non-volatile memory 24, which holds the receiver's operating system, device drivers and other software modules. The receiver's software is executed by the microprocessor):

decoding encoded images and parameters associated with the images (DECODER MANAGER of fig. 2, note Video Decoding Manager has previously received through a queue from the Overall Control a complete command ordering and specifying the decoding and/or the display of this particular picture. Based on this command, the Video Decoding Manager programs the decoding of the newly detected picture), thereby resulting in decoded images and decoder

parameters associated with the decoded images (e.g. fig. 7, note A, B, and C buffers are storing the decoded images and decoded parameters that are I2, B"3, P5 associated with the pictures) ;

storing the decoded images (A, B, and C of fig. 1);

storing indicators indicating images to be displayed in a FIFO (DISPLAY MANAGER of fig. 2) in a forward display order at normal speed (col. 6, lines 66-col. 7, line 3; note In forward mode, Next(N) returns the ID of following picture to be displayed according to normal display order (i.e. in respect to the temporal reference). In backward mode. Next(N) returns the ID of the previous picture according to normal display order); and

a second processor (14 of fig. 1) operably coupled to the queue (col. 5, line 53-col. 6, line7);

a second memory (DISPLAY MANAGER of fig. 2 for storing a software descriptor, col. 5, lines 43-46) operably coupled to the second processor (14 of fig. 1), said second memory storing a plurality of instructions (fig. 6, there are instructions) for execution by the second processor (e.g. fig. 6), wherein the plurality of executable instructions cause:

presenting the images indicated by the indicators for display (figs. 3 and 6).

Re claims 16 and 21, Abelard further discloses wherein the FIFO (DISPLAY MANAGER of fig. 2) stores the indicators (queue) in the particular order prior to the display engine displaying the images associated with the indicators in the order corresponding to the order that the indicators are stored in the FIFO (see also fig. 7).

Re claims 17-20, Abelard further discloses wherein each indicator indicates a different image to be displayed (fig. 3, I, B, or P picture is displayed; see fig. 7).

Re claim 26, Abelard further teaches wherein the queue directly transmits the indicators from the first processor to the second processor (col. 5, lines 43-46).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abelard et al. (US 7,130,526) in view of Zhou (US 6,353,700).

Re claims 22-25, Abelard teaches the display for display video pictures based on the identification, but not every picture is displayed.

However, Zhou teaches every frame is displayed after only one MPEG decoding process (col. 6, lines 39-50).

Therefore, taking the teachings of Abelard and Zhou together as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Zhou into Abelard to improve display order.

5. Applicant's arguments filed 09/03/2010 have been fully considered but they are not persuasive.

The applicant argues that Abelard does not disclose "displayed in forward order at normal speed", "wherein the queue directly transmits the indicators from the first processor to the second processor", and "every picture is displayed".

The examiner strongly disagrees with the applicant. It is submitted that Abelard discloses displayed in forward order at normal speed (col. 6, lines 66-col. 7, line 3; note In forward mode, Next(N) returns the ID of following picture to be displayed according to normal display order (i.e. in respect to the temporal reference) and wherein the queue directly transmits the indicators from the first processor to the second processor (col. 5, lines 43-46; note These descriptors are shared by the Video Decoding Manager and the Display Manager. Before programming a decoding, the Video Decoding manager tests if the reconstruction buffer that must receive this picture is available).

Zhou teaches every frame is displayed after only one MPEG decoding process (col. 6, lines 39-50).

(10) Response to Argument

I. THE CLAIMS DOES NOT COMPLY THE STATUTORY REQUIREMENTS.

A. Claims 1-19 and 22-29 do not satisfy the written description.

The written description of the specification does not disclose "**a forward order of display at normal speed**", "**every picture** is displayed" , and "wherein **the queue directly transmits the indicators** from the first processor to the second processor".

The appellant argues that the specification disclose "wherein **the queue directly transmits the indicators** from the first processor to the second processor".

The examiner strongly disagrees with the applicant. It is noted that the claims 1, 4, and 26 recite "a system for displaying images on a display, said system comprising: a decoder for decoding encoded images and parameters associated with the images, thereby resulting in

decoded images and decoded parameters associated with the decoded images; image buffers for storing the decoded images; **a FIFO for storing indicators indicating images** to be displayed in a forward display order at normal speed; and a display engine for presenting the images indicated by the FIFO for display; wherein the decoder comprises **a first processor** and the display engine comprises **a second processor**;wherein **the queue directly transmits the indicators** from **the first processor to the second processor**."

First, the claimed invention shows that the indicator is transmitted from the first processor to the FIFO, wherein the FIFO storing indicators, and then the FIFO will transmit the indicator to the second processor. This show that the indicators does not directly transmit from the first processor to the second processor.

Second, the specification [0012] shows the queue stores indicators indicating images to be displayed in the display order, and the specification [0013] shows thereby resulting in decoded images and decoder parameters associated with the decoded images, storing the decoded images, queueing indicators indicating images to be displayed. The specification [0033] discloses that at 222 the decode engine (comprises the first processor) **places an indicator at the end of the FIFO queue 130** indicating the image to be displayed **at the nearest time in the future.** The evidences above show that the indicators are stored in the FIFO and wait for the nearest time in the future and then the FIFO will transmit the indicator to the display based on a display notification. The evidences above have not shown "**the queue directly transmits the indicators** from **the first processor to the second processor**."

The appellant argues that the specification provides adequate support for **"a forward display order at normal speed"** based on MPEG and MPEG-2 standard.

The examiner strongly disagrees with the appellant. First, the appellant does not incorporate any MPEG and MPEG-2 standard in the specification by reference. There is no evidence MPEG and MPEG-2 encoded video is at **"a forward display order at normal speed"** in the specification. Second, the MPEG and MPEG-2 of the appellant presented in the appeal brief does not have any details to support the claimed language as indentified; and the specification does not show any part of the disclosure of the MPEG and MPEG-2 that discloses **"a forward display order at normal speed".** Finally, there is no association of **"a forward display order at normal speed"** with MPEG and MPEG-2 in appellant's disclosure. Furthermore, the whole appellant's argument relied on the MPEG and MPEG-2 encoded video support **"a forward display order at normal speed**". However, the appellant failed to provide any evidence from the specification and MPEG and MPEG-2 encoded video to support **"a forward display order at normal speed".**

The appellant argues that the specification support "**every picture** is displayed" relied on MPEG and MPEG-2.

The examiner strongly disagrees with the appellant. The appellant never incorporate the MPEG and MPEG-2 into the specification by reference and failed to provide details or evidences of the MPEG and MPEG-2 in the appeal brief to support "**every picture** is displayed". Neither the specification nor MPEG and MPEG-2 support " **every picture** is displayed".

II. CLAIMS 1-11, 16-21, AND 23 IS REJECTED BY ABELARD

A. Independent Claims 1, 5, 8, 11

The appellant argued that Abelard does not disclose "a decoder for decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images" and nothing in the passage as presented by the examiner discloses or suggests the decoder 9 decodes parameters associated with decoded image.

The examiner strongly disagrees with the appellant. It is submitted that Abelard discloses a decoder (9 of fig. 1) for decoding encoded images (col. 4, lines 14-20, compressed data) and parameters (DECODING MANAGER of fig. 1, there are parameters for decoding as shown in fig. 5, I, B, P parameters; wherein the decoding process is performed in figure 5 using parameters as predictors for images; col. 7, lines 30-56; If the picture identified by PicID is of "P" or "B" type, then its decoding may require the presence of forward and backward predictors; The rule that gives the predictors on which a picture to be decoded depends on is simple: going through the stream backwards (i.e. towards video access units previously recorded), the first "P" type or "i" type picture encountered is the predictor for the current picture. This picture can be found using the trickmode information. This predictor is called "NearestID" in FIG. 5) associated with the images (fig. 5, the decoding process of a picture depending on its type (I, P, or B)), thereby resulting in decoded images and decoded parameters associated with the decoded images (26 of fig. 1, A, B, and C, fig. 7; e.g. I2, P8…B0 are the decoded images stored in the memory (A, B, and C of fig. 7) and each of the images has decoded parameters associated with it). Furthermore, the decoder (9 of fig. 1) decoding the images using predictors as shown in figure 5 (col. 7, lines 30-col. 8, line 43), example B pictures are decoded require two predictors as parameters.

The appellant argued that Abelard does not disclose "a FIFO for storing indicators indicating images to be displayed in a forward display order at normal speed... ," as recited in claim 1.

The examiner strongly disagrees with the appellant. It is submitted that Abelard discloses a FIFO (VIDEO CODING MANAGER AND DISPLAY MANAGER of fig. 2, wherein the decoder transmit a queue to the decoding manager and the decoding manger will transmit a queue to the display manager, col. 5, lines 34-43) for storing indicators (Note a queue indicates the decoded picture to be displayed and how it must be displayed (Top or Bottom field)) indicating images to be displayed in a forward display order at normal speed (col 6, lines 66-col. 7, line 1, In forward mode, Next(N) returns the ID of following picture to be displayed according to normal display order (i.e. in respect to the temporal reference)).

The appellant argued that Abelard doses not discloses the "a first processor … [and] a second processor coupled to the [FIFO]..."

The examiner strongly disagrees with the appellant. It is submitted that Abelard clearly discloses "a first processor (9 of fig. 1) … [and] a second processor (14 of fig. 1) coupled to the [FIFO] (26 of fig. 1)..."

B. Claims 2, 6, 9

The appellant argued that Abelard does not disclose decoding parameters associated with the images and storing the decoded parameters.

The examiner strongly disagrees with the appellant. It is submitted that Abelard teaches the decoder (9 of fig. 1) decodes the images (fig. 5) that have parameters as predictors (col. 7, lines 30-56) and the memories A, B, and C (fig. 7) stores the images (I, P, and B) in period of

time, wherein each I, P, or B image has its own parameters herewith, for example, I has its parameter as intra and zero motion vector, P has a parameter and inter motion vector…, when the I, P, or B picture stored in the memories (A, B, or C of fig. 7), the parameters are stored herewith for the display enable to retrieve the images based on the parameters.

C. Claims 3, 7, and 10

The appellant argued that Abelard does not disclose decoding parameters associated with the images and receiving the decoded parameters and displaying the decoded image based on the decoded parameters.

The examiner strongly disagrees with the applicant. Abelard clearly discloses the I, P, and B are decoded by the process in figure 5, when the decoder (9 of fig. 1) decodes I, P, and B pictures, the decoder has to decode the decoder parameters as predictors (col. 7, lines 34-56), and the display (14 of fig. 1) displays the decoded images (I, P, and B) in period of time (fig. 7) based on the parameters (predictors), as shown in figure 7, B"3 is displayed from B memory at period 2 and frame period -4.

D. Claim 4

The appellant argues Abelard does not disclose the decoder comprises the first processor and the display comprises the second processor and there is no suggestion that the decoder 9 and processing circuit 14 are embodied in separate processors.

The examiner strongly disagrees with the appellant. It is noted that the claimed does not required the first processor and the second processor are in separate processors. Abelard discloses the decoder (9 of fig. 1) comprises the first processor (e.g. Decoding manager of fig. 2)

and processing circuitry (14 of fig. 1) comprises the second processor (e.g. Display Manager of fig. 2).

E. Claims 17-20

The appellant argued that Abelard does not disclose each indicator indicates a difference image to be displayed.

The examiner strongly disagrees with the appellant. It is submitted that each indicator indicates a difference image to be displayed (fig. 3, I, B, or P picture is display; see fig. 7. It is indicates a difference image to be displayed (fig. 3, I, B, or P picture is display; see fig. 7. It is noted that the video decoding manager programs the decoding of the newly detected picture and, if the picture must be display, notifies the display manager through a queue that this picture is to be display and how it must be displayed).

F. Claim 21

The appellant argued that does not disclose the limitation in claim 21. The examiner strongly disagrees with the appellant. Abelard discloses wherein the FIFO (DISPLAY MANAGER of fig. 2) stores the indicators (queue) in the particular order prior to the display engine displaying the images associated with the indicators in the order corresponding to the order that the indicators are stored in the FIFO (see also fig. 7).

G. Claim 26

The appellant argues that Abelard does not disclose the limitation in claim 26. The examiner strongly disagrees with the appellant. Abelard discloses wherein the queue directly transmits the indicators from the first processor to the second processor (col. 5, lines 43-46; noted that the video decoding manager programs the decoding of the newly detected picture and,

if the picture must be display, notifies the display manager through a queue that this picture is to be display and how it must be displayed).

III. CLAMS 22-25 ARE UNPATENTABLE OVER THE COMBINATION OF ABELARD AND ZHOU

A. Claims 22-25

The appellant argued that Zhou and the combination of Abelard and Zhou does not teach every picture is displayed.

The examiner strongly disagrees with the appellant. It is submitted that Abelard teaches the display (14 of fig. 1) for displaying the images (I, P, and B) in the period of time, and Zhou teaches every frame is displayed after only one MPEG decoding process (col. 6, lines 39-50). Therefore, Abelard and Zhou are combinable to make obvious claimed invention.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Tung Vo/

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/Mehrdad Dastouri/

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